TRANSISTOR-LEVEL ANALOG IC DESIGN

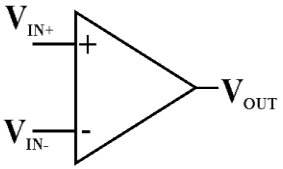
Nonlinear analog design: Comparators

A. KOUKAB
Swiss Federal Institute of Technology (EPFL)
Electronics Laboratory
1015 Lausanne- Switzerland
E_mail: maher.kayal@epfl.ch

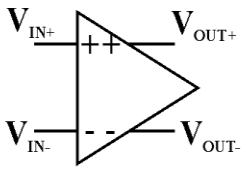
Outline

- Performance parameters (delay and resolution)
- High performances comparator
- Basic topologies
- High-speed comparators
- External and internal positive feedback
- Clocked comparator

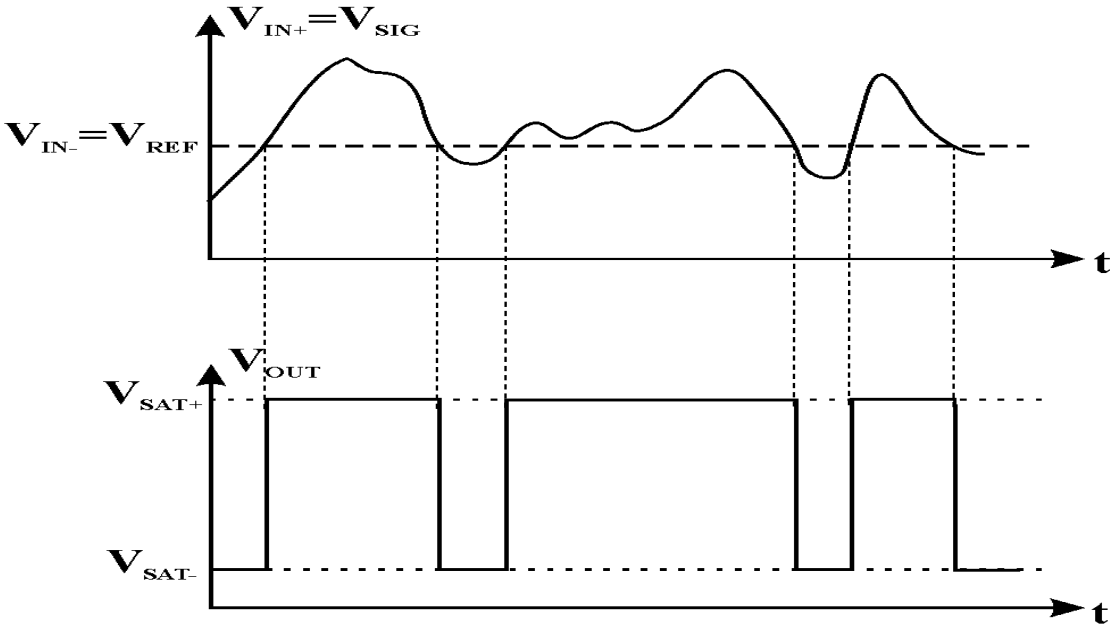
COMPARATOR

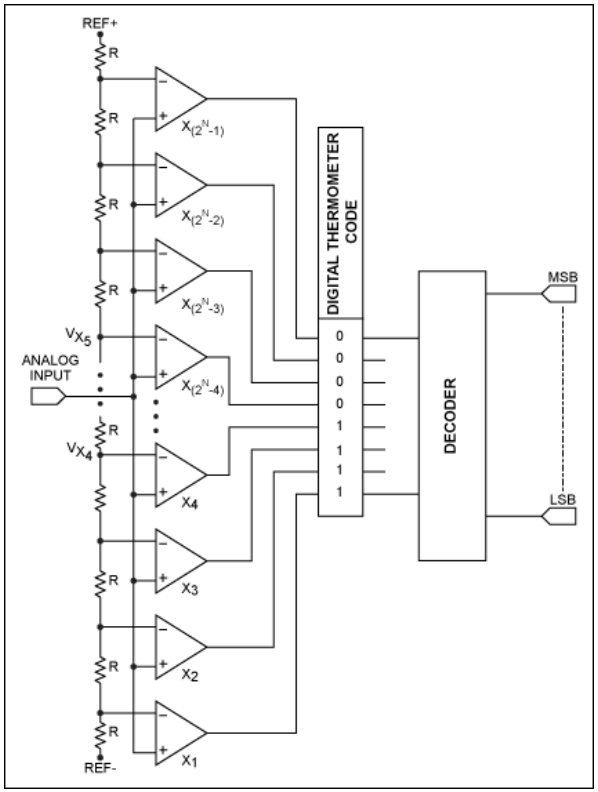


a)



b)

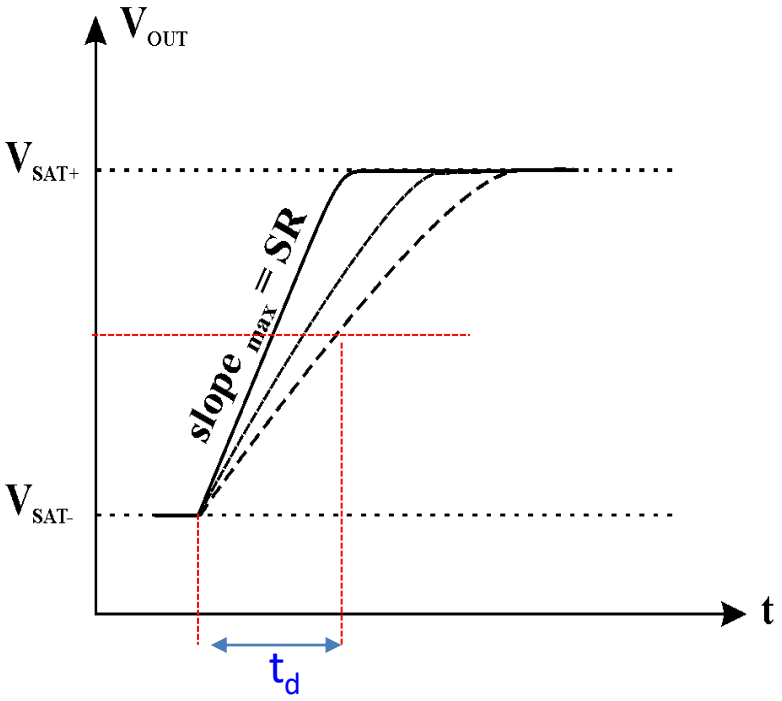




- Binary output as a result of comparison of input signal with the reference:

Performance parameters (propagation delay)

- Propagation delay t_d is the time required for the output to reach the 50% point of a transition (i.e., when ΔV_{out} reaches $(V_{SAT+}-V_{SAT-})/2$):



Jitter (noise in time domain) ↘ when td↘

- Cas1: small input change with a first-order system $\Delta V_{out}/\Delta V_{in} = A_0/(1+s\tau_1)$

$$\Delta V_{OUT}(t) = A_0 \cdot \left(1 - e^{-t/\tau_1}\right) \cdot \Delta V_{IN}$$

$$t_d = -\tau_1 \ln\left(1 - \frac{V_{SAT+} - V_{SAT-}}{2A_0 \Delta V_{IN}}\right)$$

- Case 2: Large input change

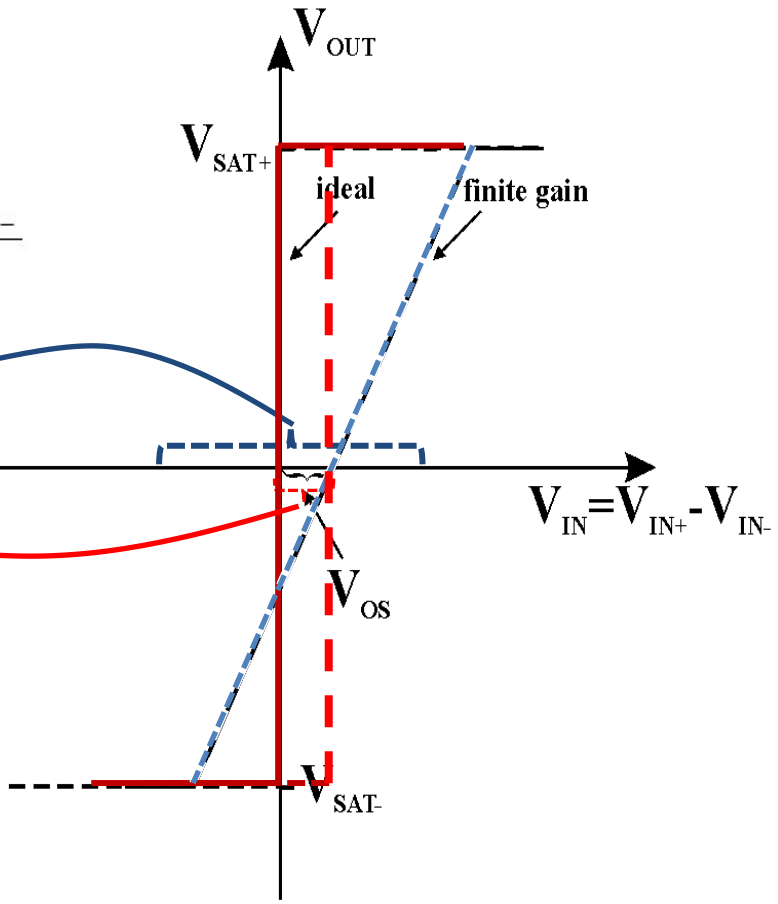
$SR = [dV_{out}/dt]_{max} = I_o/C_L$:

$$t_d = \frac{\frac{V_{SAT+} - V_{SAT-}}{2}}{\frac{I_0}{C_L}} = \frac{V_{SAT+} - V_{SAT-}}{2 \cdot SR}$$

Performance parameters: (Resolution)

- The resolution represents the minimum input difference that changes the logic value at the output state.
- It is limited by the offset and the gain variation of the comp.

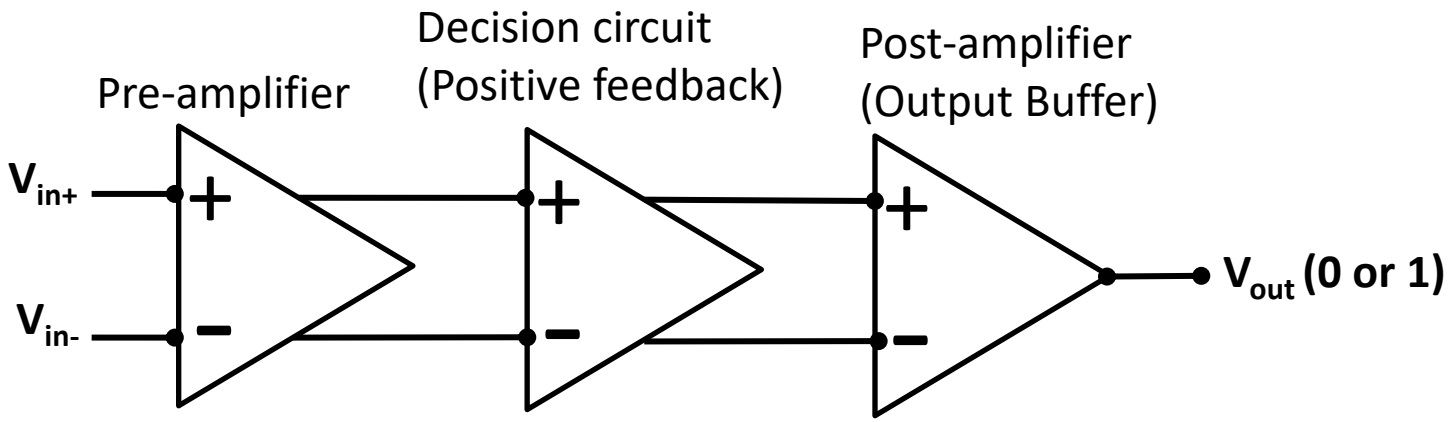
$(\Delta V_{IN})_{\min}$ given by V_{OS} and $\frac{V_{SAT+} - V_{SAT-}}{A_0}$



- Tradeoff between speed and resolution:
  - Low offset → input MOSTs in WeakInv
  - WeaInv → large transistors → Low speed

- Usually offset compensation or calibration is a mandatory in demanding comparator circuits.

High performances comparator



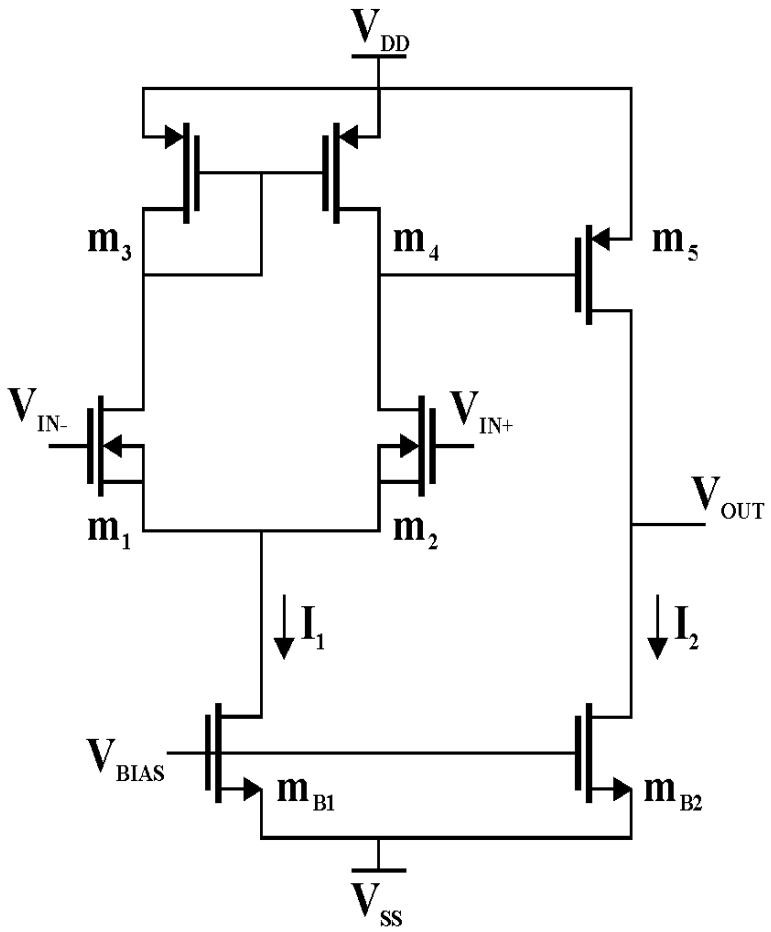
- Preamplifier:
- Amplifies the input signal to improve the comparator sensitivity;
- increases the minimum input signal with which the comparator can make a decision;
- isolates the input from switching noise coming from the positive feedback;
- usually cascade of 3 or 4 low gain-high BW amplification stages

  - Decision Circuit: determines which of the input signals is larger

  - Buffer: amplifies this information and outputs a digital signal

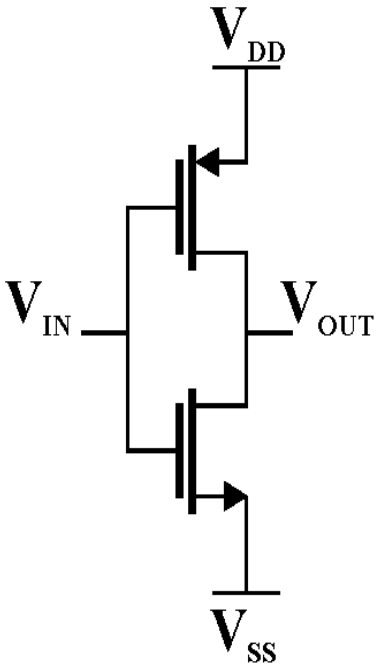
Basic topology

- Two-stage class A amplifier:



- Requires high-gain amplifiers in order to make its output saturate to the positive or negative supply rail for a small input difference (i.e., high resolution)
- No need for frequency compensation (i.e. Miller Cap)
- High Rout for high gain means High RC (i.e time constant) and high L so low Frequency transition.
- Unsuitable for high-speed and low-power applications.

Basic topology: Inverter



- if $V_{IN} < V_{T0n}$

NMOS is off, PMOS is on

$V_{out} = V_{DD}$

- if $V_{IN} > V_{DD} - V_{T0p}$

PMOS is off, NMOS is on,

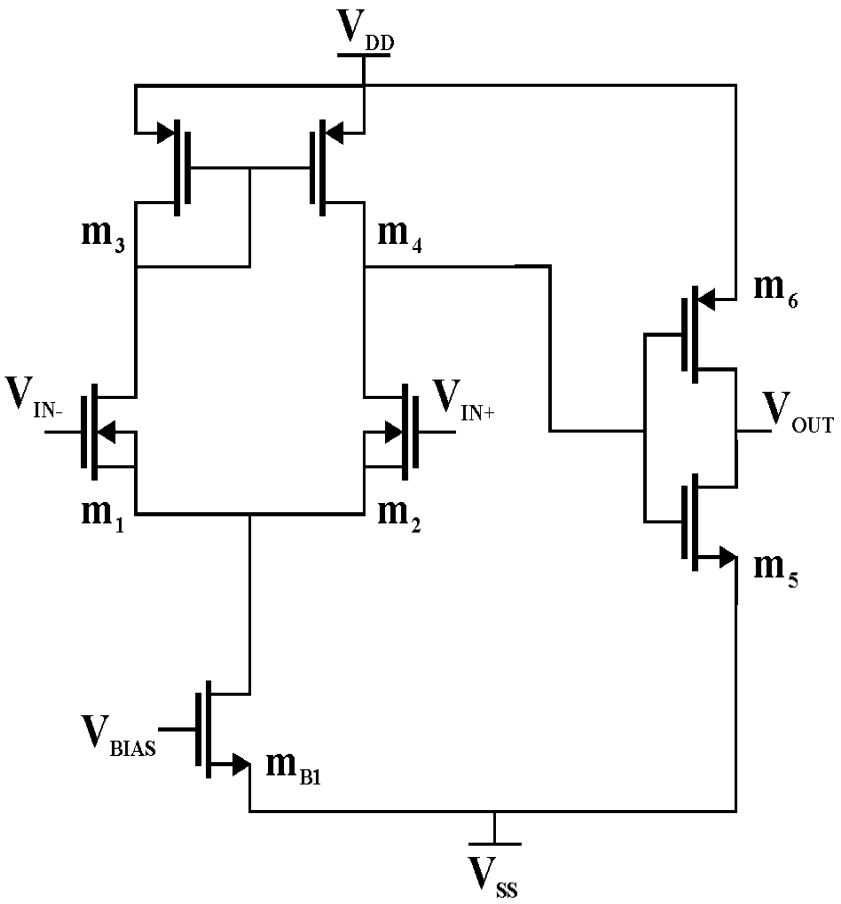
$V_{out} = V_{ss}$

- Two drawbacks:
  - V_{T0} is PVT dependent
  - if $V_{Ton} < V_{IN} < V_{DD} – V_{Top}$, Vout is not defined (NMOS is on, PMOS is on)

•To overcome this issues the inverter input signal is usually driven by a pre-amplifier (for example, a simple OTA) that amplifies the input signal of the inverter.

Basic topology 2

- Two-stage class B amplifier:

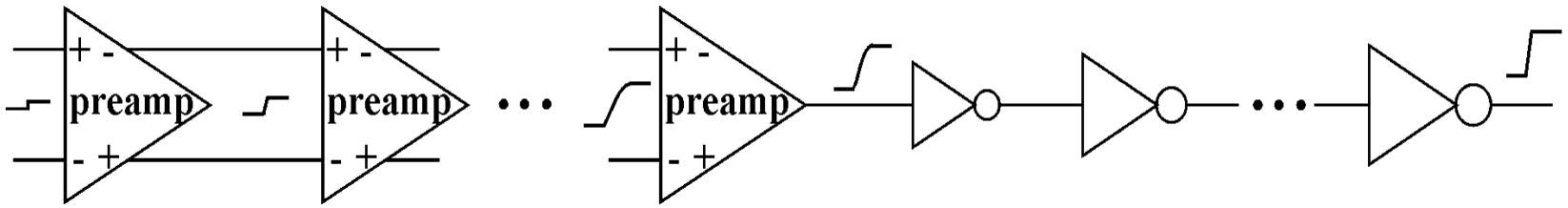


- Suitable for moderate speed and moderate power consumption.
- Output stage is class B
- Required preamplifier gain quite low: just enough to guaranty a $V_{pre} < V_{T0n}$ or $V_{pre} > V_{DD} - V_{T0p}$.
- Still PVT dependent

High-speed comparators

- Another way to realize high speed comparator is to cascade several preamplifier stages followed by several cascaded inverters or analog latches.

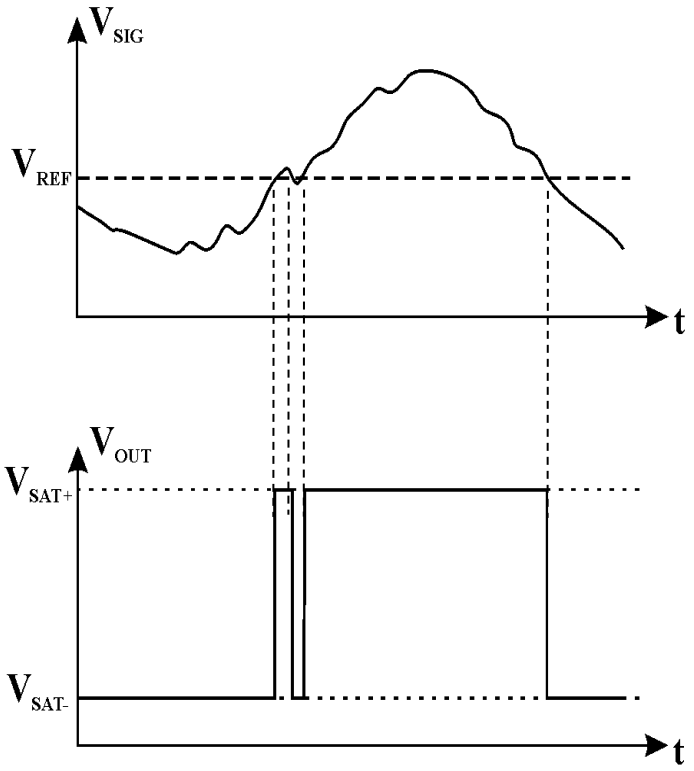
Principle illustration:



- One high gain amplifier is in general slower than several low gain amplifiers (GBW = Cst).
- Cascading several inverter stages allows to increase the load capacitance of each stage gradually without important degradation of the response time.

Basic topologies: regenerative comparators

- Comparator response in a noisy environment:

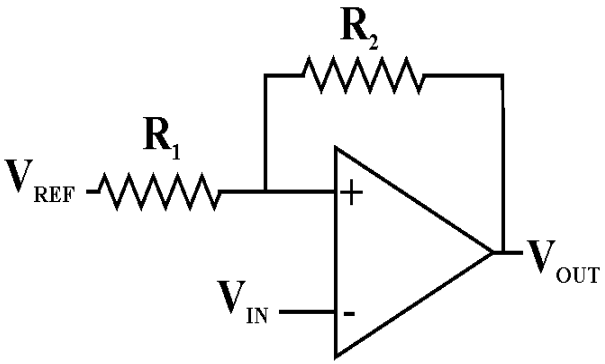


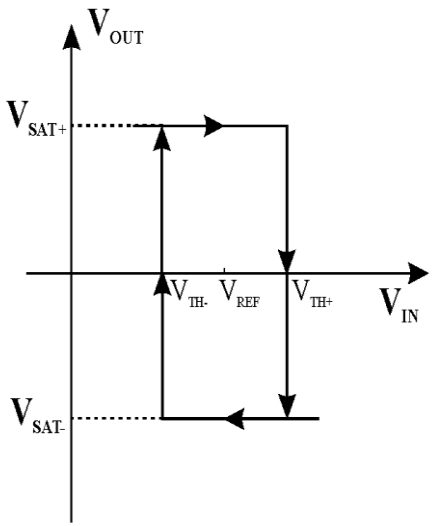
without hysteresis

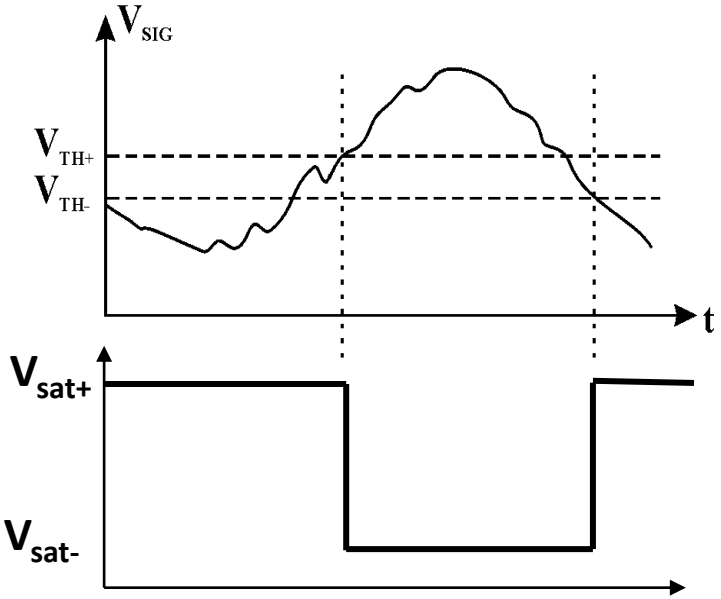
- A hysteresis is required to avoid erroneous responses.
- Hysteresis is implemented in the comparator by the use of positive (regenerative) feedback.
- The positive feedback can be external or internal.

Basic topologies: regenerative comparators

- Inverting comparator with external positive feedback:







with hysteresis

$$V_{TH+} = \left(\frac{R_1}{R_1+R_2}\right)V_{SAT+} + \left(\frac{R_2}{R_1+R_2}\right)V_{REF}$$

$$V_{TH-} = \left(\frac{R_1}{R_1+R_2}\right)V_{SAT-} + \left(\frac{R_2}{R_1+R_2}\right)V_{REF}$$

$$\Delta V_{TH} = V_{TH+} - V_{TH-} = \frac{R_1}{R_1+R_2}\left(V_{SAT+} - V_{SAT-}\right)$$

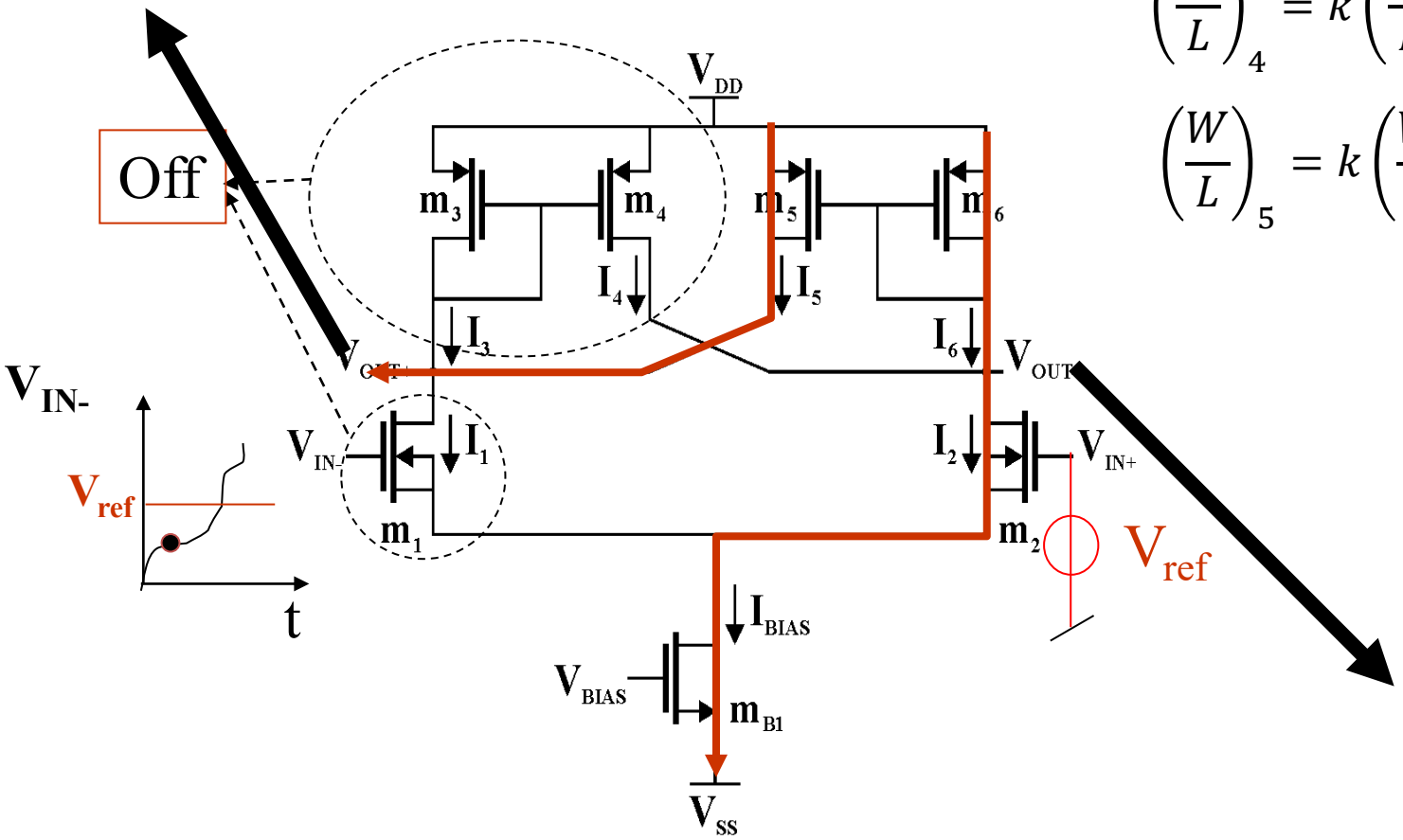
- Drawback: Resistances overload the OTA and occupy a relatively large area.
- **In ICs internal feedback is preferred**

Basic topologies: regenerative comparators

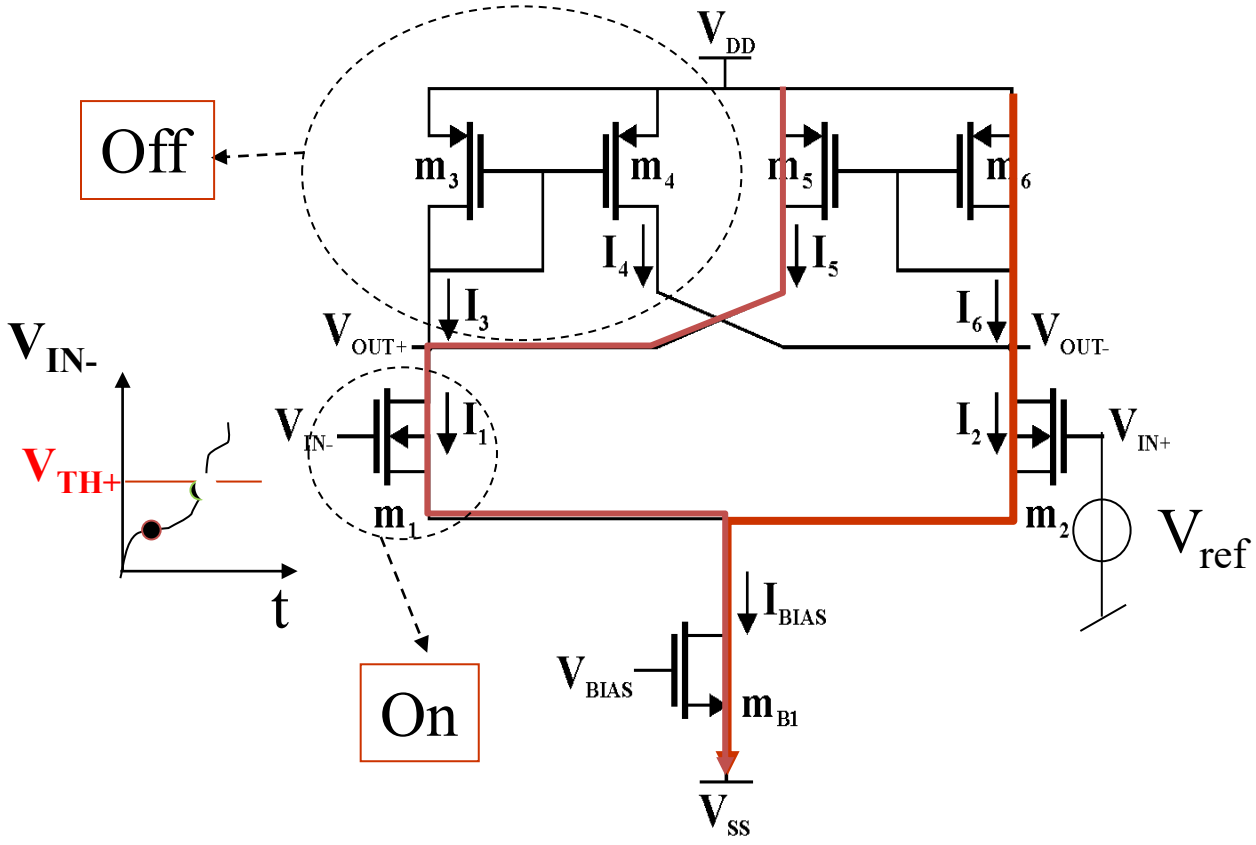
- Cross-coupled m_4 and m_5 for a Positive Feedback
- If $k \geqslant 1$ with k is the positive feedback factor

$$\left(\frac{W}{L}\right)_4 = k\left(\frac{W}{L}\right)_3$$

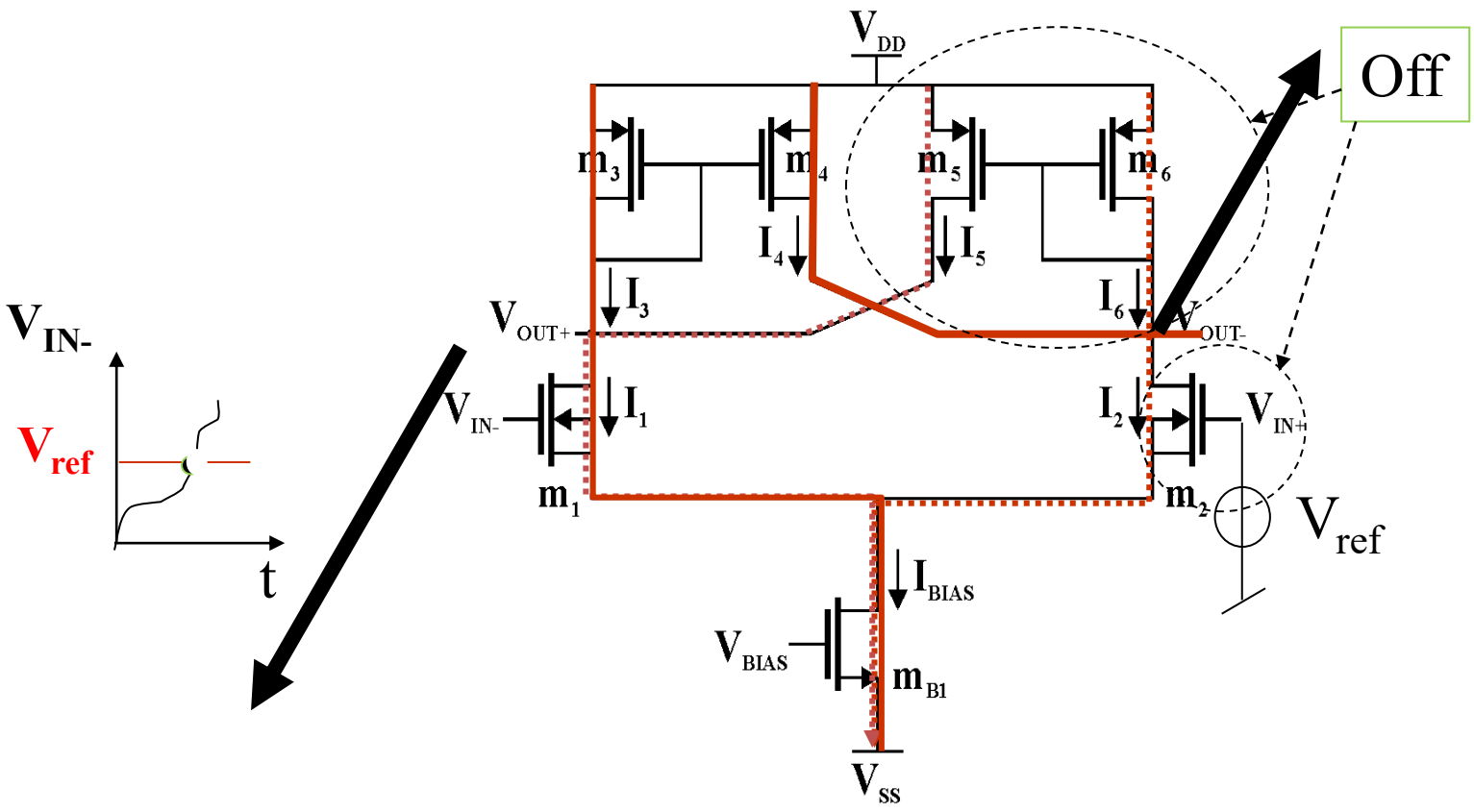
$$\left(\frac{W}{L}\right)_5 = k\left(\frac{W}{L}\right)_6$$



Switching condition



Basic topologies: regenerative comparators



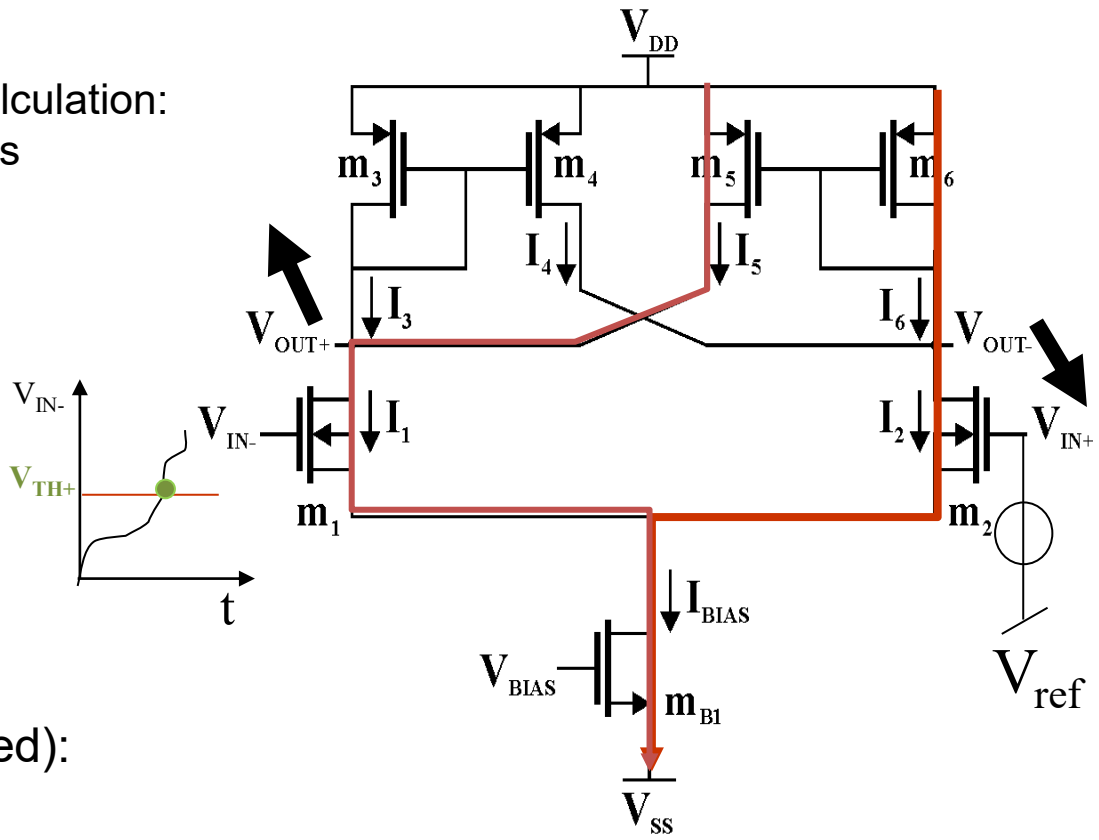
Basic topologies: regenerative comparators

- Threshold voltages V_{TH+} and V_{TH-} calculation:

Starting point just before switching states ($V_{in-}=V_{TH+}$ and V_{out+} still at V_{DD})

$$I_1 = kI_2 \quad and \quad I_1 + I_2 = I_{Bias}$$

$$\rightarrow I_2 = \frac{I_{Bias}}{1+k} \quad and \quad I_1 = \frac{kI_{Bias}}{1+k}$$



M1,2 in Strong inversion (for speed):

$$\frac{kI_{BIAS}}{1+k} = \frac{\beta_1}{2}(V_{GS1} - V_{T0})^2 \rightarrow V_{G1} = V_{T0} + \sqrt{\frac{2kI_{BIAS}}{\beta_1(1+k)}} + V_{S1}$$

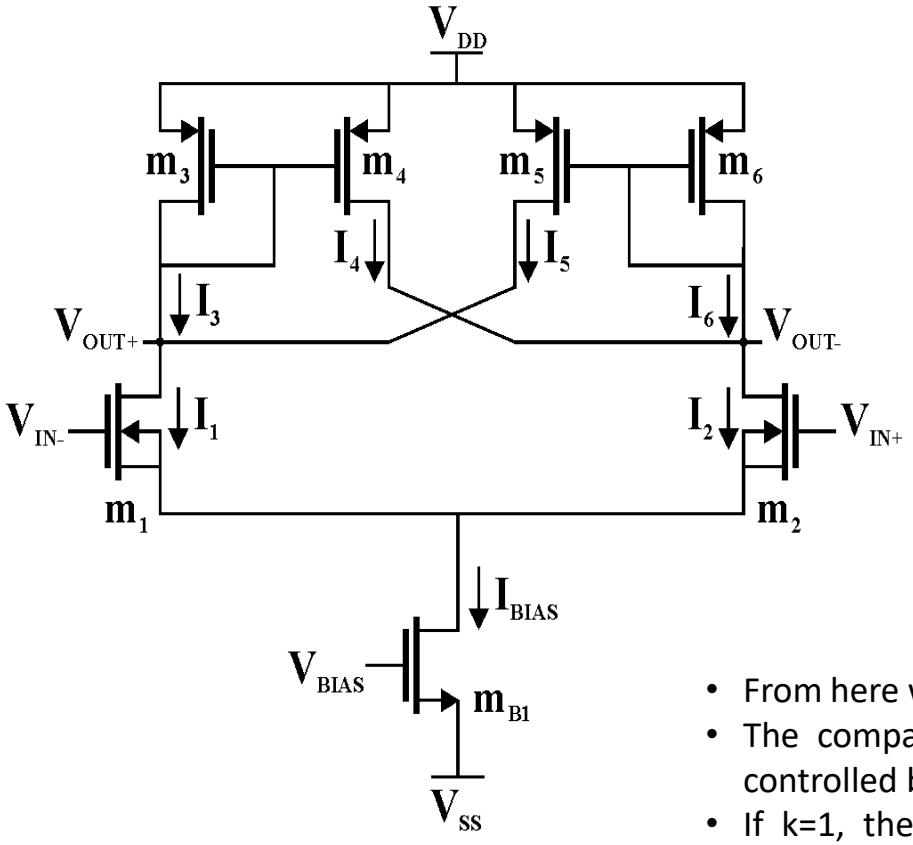
$$\frac{I_{BIAS}}{1+k} = \frac{\beta_2}{2}(V_{GS2} - V_{T0})^2 \rightarrow V_{G2} = V_{T0} + \sqrt{\frac{2I_{BIAS}}{\beta_2(1+k)}} + V_{S2}$$

$V_{G1} = V_{TH+}$, $V_{G2} = V_{ref}$, $V_{S2} = V_{S1}$

$$V_{TH+} - V_{ref} = \sqrt{\frac{2I_{BIAS}}{\beta_1(1+k)}}(\sqrt{k} - 1)$$

Basic topologies: regenerative comparators

- Inverting comparator with internal positive feedback with $\beta_1=\beta_2=\beta$ and $V_{in+}= V_{ref}$



$$V_{TH+} = V_{ref} + \sqrt{\frac{2I_{BIAS}}{\beta_1}}\left(\frac{\sqrt{k}-1}{\sqrt{1+k}}\right)$$

$$V_{TH-} = V_{ref} - \sqrt{\frac{2I_{BIAS}}{\beta_1}}\left(\frac{\sqrt{k}-1}{\sqrt{1+k}}\right)$$

$$\Delta V_{TH} = 2\sqrt{\frac{2I_{BIAS}}{\beta_1}}\left(\frac{\sqrt{k}-1}{\sqrt{1+k}}\right)$$

$$\left(\frac{W}{L}\right)_4 = k\left(\frac{W}{L}\right)_3 \qquad \left(\frac{W}{L}\right)_5 = k\left(\frac{W}{L}\right)_6$$

- From here we notice that only when k>1, the hysteresis occurs
- The comparator transfer function is clockwise and the hysteresis is controlled by the ratio k, the tail current and β of the input transistors
- If k=1, the threshold voltages are equal and there is no hysteresis (residual hysteresis due to mismatch)
- In practical realizations, the presented circuit is usually followed by an output stage (a common source or an inverter) in order to have a logic 0 or 1 (V_{ss} or V_{DD}) at the output.

Basic topologies: regenerative comparators

- Finally, if k < 1, the circuit behaves more as a gain stage with a higher speed thanks to the positive feedback.

DC analysis

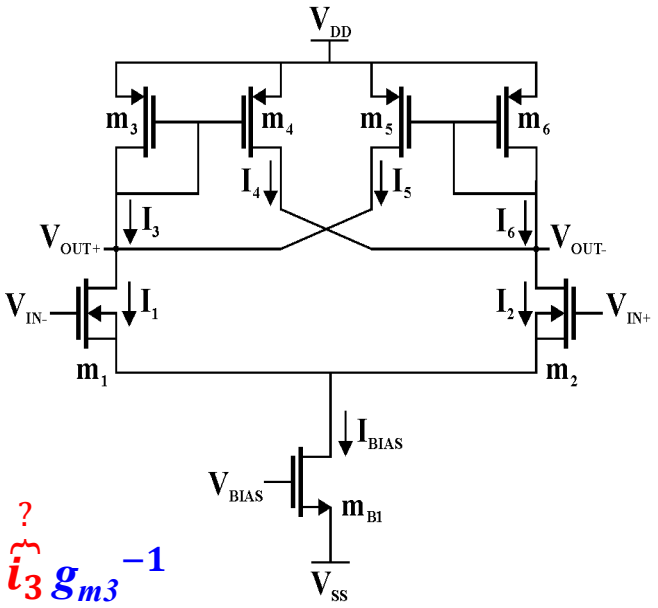
$I_1 = I_2 \rightarrow \quad g_{m1} = g_{m2}\,;\, g_{m3} = g_{m6}\,;\, g_{m4} = g_{m5}$

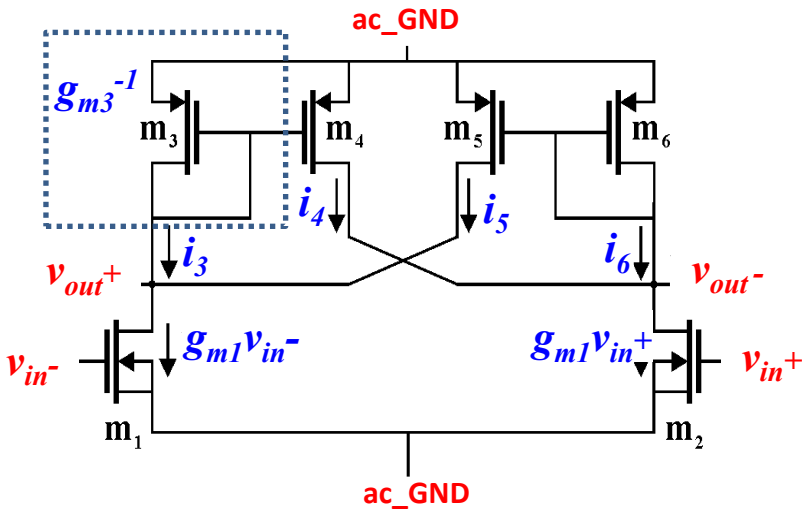
$g_{ds1} = g_{ds2}\,;\, g_{ds4} = g_{ds5}$

$I_4 = kI_3 \rightarrow \quad \mathbf{g_{m4} = k\, g_{m3}}$

ac analysis

$A_0 = \frac{v_{odif}}{v_{idif}} = ?$

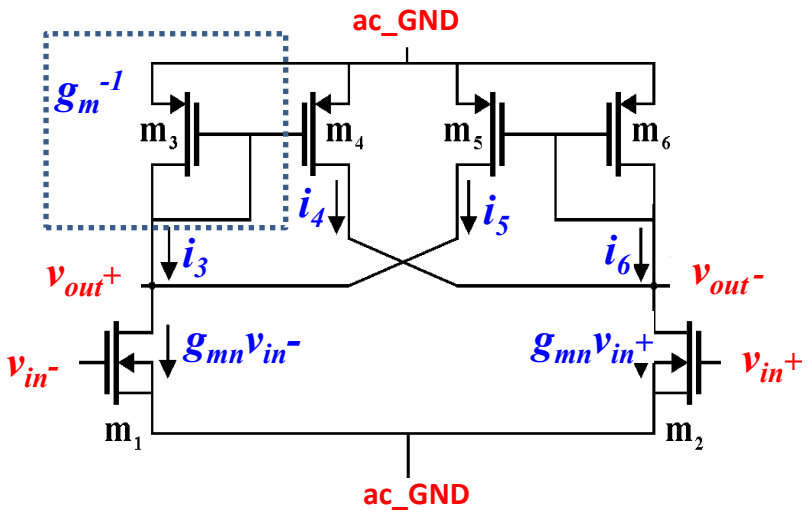




$$v_{out}^+ = -\overset{?}{i_3}\, g_{m3}^{-1}$$

$$\begin{cases} i_5 = ki_6 = -ki_3 \\ i_3 + i_5 = g_{m1}v_{in}^- \end{cases} \rightarrow \; i_3 = \frac{g_{m1}v_{in}^-}{1-k}$$

$$\rightarrow -\frac{v_{out}^+}{v_{in}^-} = \frac{v_{odif}}{v_{idif}} = A_0 = \frac{g_{m1}}{(1-k)g_{m3}}$$

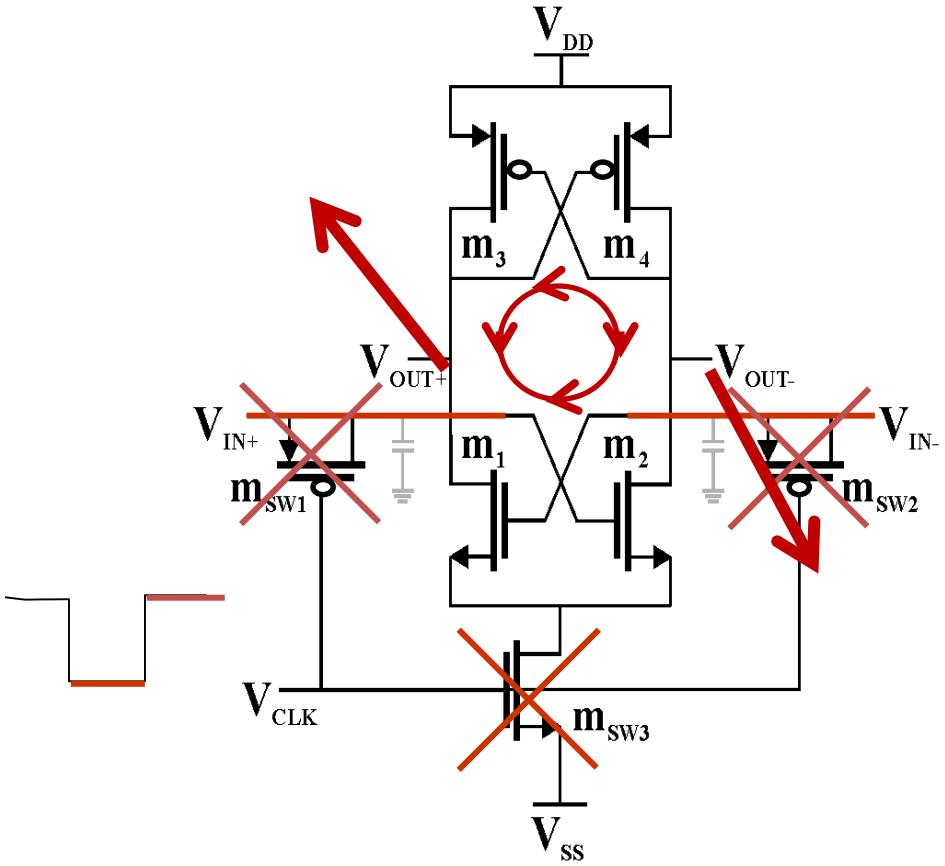


$$\begin{cases} i_5 = ki_6 = -ki_3 \\ i_3 + i_5 = g_m v_{in}^- \end{cases} \rightarrow i_3 = \frac{g_m v_{in}^-}{1-k}$$

Basic topologies: analog latch

A clocked comparator: A comparator whose outputs change on the rising (or falling) edge of a clock (Sample, Hold and compare).

Case: $V_{in+} > V_{in-}$



Warning: Charge injection, switching noise of the positive feedback

Need to isolate the inputs (i.e. use a preamplifier)